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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,937	09/06/2000	Jong Sang Baek	8733.289.00	8624

30827 7590 05/09/2002

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ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 05/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/655,937	Applicant(s) Baek et al.
	Examiner Alecia Nelson	Art Unit 2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 6, 2000* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☒ Claims *1-21* are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), which papers have been made of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. ***Claims 1, 2, 4, 6, 8, 9, 11, and 20***, are rejected under 35 U.S.C. 102(e) as being anticipated by Shin (U.S. Patent No. 6,323,836).

With reference to **claims 1, 8, and 20**, Shin teaches a liquid crystal display device (100), comprising a line memory (230) for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups; a driving circuit (270) including n driver integrated circuits (240, 250) that are connected to the line memory (230) and the liquid crystal display panel (100) to drive the liquid crystal display panel in response to the data outputted from the line memory

(230); and a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every period of the data clock in response to a time corresponding to the number of said groups (see column 5, line 18-column 6, line 18). With further reference to **claims 8 and 20**, Shin teaches, with reference to the summary of the invention, generating a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of divided groups (see column 3, lines 53-62).

With reference to **claims 2 and 9**, Shin teaches, with reference to FIG. 4, a first group (A) and a second group (B), wherein the data driver ICs are divided also into the two groups (A, B) and the video data are sent to and latched at the two groups (see col. 2, lines 43-54).

With reference to claim with reference to **claims 4, 6, and 11**, Shin teaches, with reference to FIG 5, that the data driver ICs are divided into two groups. One group, an odd data driver IC group (32), is the driver for ICs connected with the odd numbered data lines. The other group, an even data driver IC group (33), is for the driver ICs connected to the even numbered data lines (see column 2, lines 56-64).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. ***Claims 3, 5, 7, 10, 12 and 21*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin as applied to **claims 1 and 20** above, and further in view of Park (U.S. Patent No. 6,040,828).

With reference to **claims 3, 5, 7, 10, and 12** Shin fails to specifically teach the timing controller generates an inverted data clock having a phase contrary to the input data clock.

Park teaches a liquid crystal display device wherein the driving circuit includes a clock generator processing a first clock signal to output a second clock signal, the clock speed of the

second clock signal being half of that of the first clock signal, a memory for storing a first video data and a second video data in accordance with the first clock signal, and a data controller for simultaneously outputting the first video data and the second video data stored in the memory in accordance with the second clock signal (see abstract). There is also taught that a gate shift clock (GSC) signal is input of the shift registers (SR-SRn) and the logic gates (AND1-AND2n) are AND gates which are alternatively applied with the GSC signal and with the inverted gate shift clock (GSC') signal. When the GSC signal and its inverted signal GSC' are synchronously applied, the gate (G1) is driven during the positive trigger of the gate shift clock signal GSC, and the gate (G2) is driven during the positive trigger of the inverted signal GSC' of the GSC signal. Consequently, two corresponding gate pulses of the gate driver IC are sequentially enabled in a horizontally synchronous interval (see column 5, lines 1-34).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to include an two clock signals, one having a phase contrary to the input data clock, as taught by Park, in a system similar to that which is taught by Shin, in order to provide a liquid crystal device in which the video data of two data lines can be driven thereby improving the display quality of the liquid crystal display.

6. ***Claims 13-19*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Parks.

With reference to claims 13 and 18 Shin teaches a liquid crystal display device (100), comprising a line memory (230) for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups; a driving circuit (270) including n driver integrated circuits (240, 250) that are connected to the line memory (230) and the liquid crystal display panel (100) to drive the liquid crystal display panel in response to the data outputted from the line memory (230); and a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every period of the data clock in response to a time corresponding to the number of said groups (see column 5, line 18-column 6, line 18). Shin further teaches, with reference to the summary of the invention, generating a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of divided groups (see column 3, lines 53-62). With further reference to **claim 14**, Shin teaches, with reference to FIG. 4, a first group (A) and a second group (B), wherein the data driver ICs are divided also into the two groups (A, B) and the video data are sent to and latched at the two groups (see col. 2, lines 43-54). With reference to **claim 16**, Shin teaches, with reference to FIG 5, that the data driver ICS are divided into two groups. One group, an odd data driver IC group (32), is the driver for ICS connected with the odd numbered data lines. The other group, an even data driver IC group (33), is for the driver ICs connected to the even numbered data lines (see column 2, lines 56-64).

Shin fails to specifically teach outputting two pixel data in each of the groups to the driving circuit during each period of the first data clock. However, Shin does teach that the divided driving method is commonly used for high resolution LCD as well (see column 2, line 65-column 3, line 2).

With further reference to **claims 15, 17, and 19**, Park teaches a liquid crystal display device wherein the driving circuit includes a clock generator processing a first clock signal to output a second clock signal, the clock speed of the second clock signal being half of that of the first clock signal, a memory for storing a first video data and a second video data in accordance with the first clock signal, and a data controller for simultaneously outputting the first video data and the second video data stored in the memory in accordance with the second clock signal (see abstract). There is also taught that a gate shift clock (GSC) signal is input of the shift registers (SR-SRn) and the logic gates (AND1-AND2n) are AND gates which are alternatively applied with the GSC signal and with the inverted gate shift clock (GSC') signal. When the GSC signal and its inverted signal GSC' are synchronously applied, the gate (G1) is driven during the positive trigger of the gate shift clock signal GSC, and the gate (G2) is driven during the positive trigger of the inverted signal GSC' of the GSC signal. Consequently, two corresponding gate pulses of the gate driver IC are sequentially enabled in a horizontally synchronous interval (see column 5, lines 1-34).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to include an two clock signals, one having a phase contrary to the input data clock,

as taught by Park, in a system similar to that which is taught by Shin, in order to provide a liquid crystal device in which the video data of two data lines can be driven thereby improving the display quality of the liquid crystal display.

Conclusion

7. Any response to this action should be mailed to: Commissioner of Patents and Trademarks Washington, D.C. 2023; or faxed to: (703) 308-9051, (for formal communications intended for entry) or: (703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT"). Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143 between the hours of 8:00 a.m and 5:00 p.m. on Monday-Friday.

If attempts to reach the above examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703)305-9720.

adn/ADN
May 2, 2002

DENNIS-DOON CHOW
PRIMARY EXAMINER